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1 **Fat tree encoder design for ultra-high speed flash A/D converters**
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2 **A novel coding scheme for the ROM of parallel ADCs, featuring redu conversion noise in the case of single bubbles in the thermometer cod**
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[Abstract] [PDF Full-Text (616 KB)] IEEE CNF

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5 **A CMOS 6-b, 400-MSample/s ADC with error correction**
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[Abstract] [PDF Full-Text (344 KB)] IEEE JNL

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8 **The design of 8-bit CMOS digital to analog converter**
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13 **A cellular nonlinear network for digital error correction**
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14 **Pseudo C-2C ladder-based data converter technique**
Lin Cong;
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15 **Digital pulse width modulator architectures**
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Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th
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1 Designing large real-time systems with Ada
Kjell W. Nielsen, Ken Shumate
August 1987 **Communications of the ACM**, Volume 30 Issue 8

Full text available: pdf(1.84 MB) Additional Information: full citation, abstract, references, citings, index terms, review

The programming language Ada encourages improved methods for the design of real-time systems.

2 BGRAF2: a real-time graphics language with modular objects and implicit dynamics
S. Bergman, A. Kaufman
July 1976 **ACM SIGGRAPH Computer Graphics , Proceedings of the 3rd annual conference on Computer graphics and interactive techniques**, Volume 10 Issue 2

Full text available: pdf(121.22 KB) Additional Information: full citation, abstract, references, citings

The BGRAF2 language for interactive real-time 2D graphics was designed as a user-oriented language emphasizing ease of use rather than of implementation. Procedural statements allow straightforward computation while classlike characteristics encourage modular graphics programming. The clock and event data types facilitate creation of parallel and synchronous procedures automatically acting on structures and display files. A graphic procedure, which includes procedural, drawing and event-driven s ...

3 Analog synthesis & design methodology: Systematic design of a 200 MS/s 8-bit interpolating/averaging A/D converter
J. Vandenbussche, K. Uyttenhove, E. Lauwers, M. Steyaert, G. Gielen
June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(993.97 KB) Additional Information: full citation, abstract, references, index terms

The systematic design of a high-speed, high-accuracy Nyquist-rate A/D converter is proposed. The presented design methodology covers the complete flow and is supported by software tools. A generic behavioral model is used to explore the A/D converter's specifications during high-level design and exploration. The inputs to the flow are the specifications of the A/D converter and the technology process. The result is a generated layout and the corresponding extracted behavioral model. The approach ...

Keywords: A/D converters, flash, interpolating, simulated annealing

4 Toward a real-time Ada design methodology
Norman R. Howes
December 1990 **Proceedings of the conference on TRI-ADA '90**
Full text available: pdf(1.63 MB) Additional Information: full citation, references, citings

5 VLSI in the nanometer era: CMOS flash analog-to-digital converter for high speed and low voltage applications
Jincheol Yoo, Kyusun Choi, Jahan Ghaznavi
April 2003 **Proceedings of the 13th ACM Great Lakes symposium on VLSI**
Full text available: pdf(523.22 KB) Additional Information: full citation, abstract, references, index terms

A CMOS flash analog-to-digital converter (ADC) designed for high speed and low voltage is presented. Using the Threshold Inverter Quantization (TIQ) comparator technique, a flash ADC can be applied to low supply voltage. A fat tree encoder that has signal delay of *O(log2 N)* is used for performance. A 6-bit and an 8-bit flash ADC were designed with 0.07 *mμ* CMOS technology and 0.7 *V* power supply voltage. The 6-bit ADC operates up to 4.76 giga samples per ...

Keywords: TIQ comparator, analog-to-digital converter, fat tree encoder, flash ADC, high speed, low voltage

6 Low power converter circuits: A low-power rail-to-rail 6-bit flash ADC based on a novel complementary average-value approach
Hui-Chin Tseng, Hsin-Hung Ou, Chi-Sheng Lin, Bin-Da Liu
August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**
Full text available: pdf(286.33 KB) Additional Information: full citation, abstract, references, index terms

In this paper, a 6-bit 300-MSample/s(MS/s) flash analog-to-digital converter (ADC) with a novel complementary average-value (CAV) approach is proposed. Input signal is pre-processed and then steered to be compared with a fixed reference voltage level, which greatly simplifies the comparator design and thus power consumption is reduced. In addition, rail-to-rail input range can be achieved by the proposed CAV technique, and the offset as well as bubble errors can therefore be minimized as a resul ...

Keywords: CMOS analog circuit, comparator, flash analog-to-digital converter, low power, rail-to-rail

7 Implementing constraint imperative programming languages: the Kaleidoscope'93 virtual machine
Gus Lopez, Bjorn Freeman-Benson, Alan Borning
October 1994 **ACM SIGPLAN Notices , Proceedings of the ninth annual conference on Object-oriented programming systems, language, and applications**, Volume 29 Issue 10
Full text available: pdf(1.59 MB) Additional Information: full citation, abstract, references, index terms

Constraint Imperative Programming (CIP) languages integrate declarative constraints with imperative state and destructive assignment, yielding a powerful new programming paradigm. However, CIP languages are difficult to implement efficiently due to complex interactions between the two donor paradigms. Neither the virtual machines for classical object-oriented languages, nor those for existing constraint languages, are suitable for implementing CIP languages, as each assumes a purely impera ...

Keywords: constraint imperative programming, constraints, incremental constraint solving, virtual machines

8 Defect-oriented test methodology for complex mixed-signal circuits
F. C. M. Kuijstermans, M. Sachdev, A. P. Thijssen
March 1995 **Proceedings of the 1995 European conference on Design and Test**
Full text available: pdf(660.89 KB) Publisher Site Additional Information: full citation, abstract

Testing of analog blocks in digital circuits is emerging as a critical factor in the success of mixed-signal ICs. The present specification-oriented testing of these blocks results in high test costs and doesn't ensure detection of all defects, causing potential reliability problems. To solve these problems, in this paper a defect-oriented test methodology for mixed analog-digital circuits is proposed. The strength of the method is demonstrated by an implementation for a complex mixed-signal cir ...

Keywords: CMOS, CMOS integrated circuits, DfT guidelines, analogue-digital conversion, complex mixed-signal circuits, defect coverage, defect-oriented test methodology, design for testability, flash analog-to-digital converter, integrated circuit testing, mixed analog-digital circuits, mixed analogue-digital integrated circuits, test costs

9 (Special session) presentation + poster disscussion: university design contest: A dynamic element matching circuit for multi-bit delta-sigma modulators
Ryozo Katoh, Shin-ya Kobayashi, Takao Waho
January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair 2004**
Full text available: pdf(161.73 KB) Additional Information: full citation, abstract, references

A 30k-gate dynamic element matching circuit for bandpass modulators with a 4-bit quantizer is designed by using 0.35-μm CMOS technology. Second-order bandpass mismatch-shaping algorithm improves the signal-to-noise ratio by ~30dB (~5 bit). The core circuit area and the estimated operation speed were 1.44 mm^2 and 20 MHz, respectively.

10 Advances in analog circuit and layout synthesis: Correct-by-construction layout-centric retargeting of large analog designs
Sambuddha Bhattacharya, Nuttorn Jangkrajarng, Roy Hartono, C.-J. Richard Shi
June 2004 **Proceedings of the 41st annual conference on Design automation**
Full text available: pdf(810.00 KB) Additional Information: full citation, abstract, references, index terms

Aggressive design cycles in the semiconductor industry demand a design-reuse principle for analog circuits. The strong impact of layout intricacies on analog circuit performance necessitates design reuse with special focus on layout aspects. This paper presents a computer-aided design tool and the methodology for a layout-centric reuse of large analog intellectual-property blocks. From an existing layout representation, an analog circuit is retargeted to different processes and performances; the ...

Keywords: analog integrated circuit design, analog layout automation, analog synthesis and optimization, layout symmetry

11 Interconnect in communication networks: NoCIC: a spice-based interconnect planning tool emphasizing aggressive on-chip interconnect circuit methods
Vishak Venkatraman, Andrew Laffely, Jinwook Jang, Hempraveen Kukkamalla, Zhi Zhu, Wayne

Burleson
February 2004 **Proceedings of the 2004 international workshop on System level interconnect prediction**
Full text available: pdf(355.87 KB) Additional Information: full citation, abstract, references, index terms

Performance and power of on-chip interconnects in the nanometer realm have been an increasing source of concern to designers. Network-on-Chip (NoC)structures have been proposed as a solution to achieve efficient and reliable communication. Even with the regularity of NoC structures, it is important for designers to acknowledge the physical layer interconnect issues to plan and quantify achievable performance. In this paper we present a spice-based tool: *No-CIC: Network-on-Chip Interconnect Ca ...*

Keywords: *interconnects, network-on-chip, on-chip, signaling, spice-based*

12 Engineering component-based net-centric systems for embedded applications
Jens H. Jahnke
September 2001 **ACM SIGSOFT Software Engineering Notes , Proceedings of the 8th European software engineering conference held jointly with 9th ACM SIGSOFT international symposium on Foundations of software engineering**, Volume 26 Issue 5
Full text available: pdf(1.39 MB) Additional Information: full citation, abstract, references, citings, index terms

The omnipresence of the Internet and the World Wide Web (Web) via phone lines, cable-TV, power lines, and wireless RF devices has created an inexpensive media for telemonitoring and remotely controlling distributed electronic appliances. The great variety of potential benefits of aggregating and connecting embedded systems over the Internet is matched by the currently unsolved problem of how to design, test, maintain, and evolve such heterogeneous, collaborative systems. Recently, component-orie ...

Keywords: SDL, component-oriented development, embedded softare, network-centric computing

13 Itanium processor clock design
Utpal Desai, Simon Tam, Robert Kim, Ji Zhang, Stefan Rusu
May 2000 **Proceedings of the 2000 international symposium on Physical design**
Full text available: pdf(117.47 KB) Additional Information: full citation, references

Keywords: IA-64, Itanium processor, clock distribution, deskew, on-die-clock-shrink

14 Systematic Design of a 200 Ms/S 8-bit Interpolating A/D Converter
J. Vandenbussche, E. Lauwers, K. Uyttenhove, M. Steyaert, G. Gielen
March 2002 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(1.34 MB) Additional Information: full citation, abstract
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The systematic design of a high-speed, high-accuracyNyquist A/D converter is proposed. The presented designmethodology covers the complete flow and is supported bysoftware tools. A generic behavioral model is used toexplore the A/D converter's specifications during high-leveldesign and exploration. The inputs are thespecifications of the A/D converter and the technologyprocess. The result is a generated layout and thecorresponding extracted behavioral model. The approachhas been applied to a rea ...

15 Language constructs and support systems for distributed computing
C. S. Ellis, J. A. Feldman, J. E. Heliotis
August 1982 **Proceedings of the first ACM SIGACT-SIGOPS symposium on Principles of distributed computing**
Full text available: pdf(850.82 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes programming constructs and system support functions that are intended to facilitate the programming of reliable distributed systems. The systems considered include very different kinds of computers communicating through a network. Such a heterogeneous network offers a number of advantages to designers of applications software. Different machines emphasize different capabilities and many problems naturally break down into subproblems that are best solved with specialized ...

16 Session 14: middleware support for multimedia: A pluggable service-to-service communication mechanism for home multimedia networks
Jin Nakazawa, Hideyuki Tokuda
December 2002 **Proceedings of the tenth ACM international conference on Multimedia**
Full text available: pdf(436.61 KB) Additional Information: full citation, abstract, references

This paper proposes a pluggable service-to-service (S2S) communication mechanism in a middleware for home networks, called Virtual Networked Appliance (VNA) architecture. In the architecture, service description method and the plug-gable S2S communication mechanism are separated in an orthogonal way. Through the separation, VNA architecture solved problems of home networks on which users have to operate multiple heterogeneous middleware technologies simultaneously: middleware fragmentation probl ...

17 Behavioral simulation for noise in mixed-mode sampled-data systems
Edward W. Y. Liu, Alberto L. Sangiovanni-Vincentelli
November 1992 **Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(514.16 KB) Additional Information: full citation, references, citings, index terms

18 The programmers' playground: a demonstration
Kenneth J. Goldman, T. Paul McCartney, Ram Sethuraman, Bala Swaminathan
January 1995 **Proceedings of the third ACM international conference on Multimedia**
Full text available: htm(12.51 KB) Additional Information: full citation, references, index terms

Keywords: direct manipulation, distributed computing, graphical user interfaces, multimedia, reconfiguration, user interface management system

19 Transportable Applications Environment (TAE) Plus user interface designer WorkBench
Martha R. Szczur
June 1992 **Proceedings of the SIGCHI conference on Human factors in computing systems**
Full text available: pdf(294.22 KB) Additional Information: full citation, abstract, references, citings, index terms

TAE Plus was built at NASA's Goddard Space Flight Center to support the building of GUI

user interfaces for highly interactive applications, such as realtime processing systems and scientific analysis system. TAE Plus is designed as a productivity tool for the user interface designer. Human factor experts and user interface designers frequently do not want to have to learn the programming details of the windowing environment before they use a GUI development tool to prototype and/or develop ...

Keywords: design tools, development tools, productivity, user interface, user interface management system

20 Is it live or is it Memorex?

Tory Sawyer, Randy Anderson, Gary McCuaig
September 1986 **Proceedings of the 14th annual ACM SIGUCCS conference on User services: setting the direction**
Full text available: pdf(2.60 MB) Additional Information: full citation, index terms

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